What is claimed is:

1. A phase-locked loop bandwidth calibration circuit, comprising:

a programmable charge pump;

a phase-locked loop filter operatively connected to said programmable charge pump;

an oscillator, operatively connected to said phase-locked loop filter, to generate a frequency signal based upon a signal received from said phase-locked loop filter; and

a control loop operatively connected to said phase-locked loop filter and said programmable charge pump;

said control loop controlling said programmable charge pump to adjust its output current level based on a measured gain of said oscillator.

2. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said control loop includes a voltage measurement circuit, operatively connected to said phase-locked loop filter, to measure a voltage being output from said phase-locked loop filter; an analog to digital converter, operatively connected to said voltage measurement circuit, to convert the measured voltage into a digital signal; and a controller to cause said programmable charge pump to adjust its output current level based upon a received digital signal from said analog to digital converter.

3. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said control loop controls said programmable charge pump to adjust its output

current level so that the product of the measured gain and a charge pump current level is kept constant.

4. The phase-locked loop bandwidth calibration circuit as claimed in claim 2, further comprising:

a voltage reference circuit, operatively connected to said programmable charge pump and said analog to digital converter, to generate and apply a same reference voltage to said programmable charge pump and said analog to digital converter based upon changes in a bandgap voltage.

5. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, further comprising:

an integer-N divider operatively connected to an output of said oscillator; and

a phase and frequency detector operatively connected between said integer-N divider and said programmable charge pump.

6. The phase-locked loop bandwidth calibration circuit as claimed in claim 5, wherein said control loop controls said programmable charge circuit to adjust its output current level so that the product of the measured gain and a charge pump current level divided by an average N value, said N value being provided by said integer-N divider, is kept constant.

7. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, further comprising:

an integer-N divider operatively connected to an output of said oscillator;

a sigma-delta-modulator operatively connected to said integer-N divider; and

a phase and frequency detector operatively connected between said integer-N divider and said programmable charge pump.

8. The phase-locked loop bandwidth calibration circuit as claimed in claim 7, wherein said control loop controls said programmable charge pump to adjust its output current level so that the product of the measured gain and a charge pump current level divided by an average N value, said N value being provided by said integer-N divider, is kept constant.

9. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, further comprising:

a programmable gain amplifier to receive either a signal from a calibration signal;

a comparator for comparing a voltage of an output from said programmable gain amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator to produce a gain signal; and

a gain controller, in response to said gain signal produced by said comparator, to control a gain of said programmable gain amplifier.

10. The phase-locked loop bandwidth calibration circuit as claimed in claim 9, wherein said gain controller includes a counter and a plurality of resistors, said plurality of resistors being switchable into or out of a circuit connected between an output of said programmable gain amplifier and an input of said programmable gain amplifier.

11. The phase-locked loop bandwidth calibration circuit as claimed in claim 9, wherein said gain controller controls the gain of said programmable gain amplifier such that a full scale input to said programmable gain amplifier produces said predetermined frequency shift in said oscillator.

12. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said capacitor to a voltage of said phase-locked loop filter; and a switch to switch said capacitor into the phase-locked loop filter circuit to effect a phase-locked loop bandwidth.

13. The phase-locked loop bandwidth calibration circuit as claimed in claim 1, wherein said phase-locked loop filter includes a dual path having an integrator path and a lead-lag path.

14. The phase-locked loop bandwidth calibration circuit as claimed in claim 13, wherein said programmable charge pump provides a first current output level to said integrator path and a second current output level to said lead-lag path.

15. A phase-locked loop circuit, comprising:

a programmable charge pump;

a phase-locked loop filter operatively connected to said programmable charge pump; and

an oscillator, operatively connected to said phase-locked loop filter, to generate a frequency signal based upon a signal received from said phase-locked loop filter;

said programmable charge pump having a resistive value;

said phase-locked loop filter having a resistive value;

said resistive value of said programmable charge pump being matched to said resistive value of said phase-locked loop filter.

16. The phase-locked loop circuit as claimed in claim 15, further comprising:

a control loop operatively connected to said phase-locked loop filter and said programmable charge pump;

said control loop controlling said programmable charge pump to adjust its output current level based on a measured gain of said oscillator.

17. The phase-locked loop circuit as claimed in claim 16, wherein said control loop includes a voltage measurement circuit, operatively connected to said phase-locked loop filter, to measure a voltage being output from said phase-locked loop filter; an analog to digital converter, operatively connected to said voltage measurement circuit, to convert the measured voltage into a digital signal; and a controller to cause said programmable charge pump to adjust its output current level based upon a received digital signal from said analog to digital converter.

18. The phase-locked loop circuit as claimed in claim 16, wherein said control loop controls said programmable charge pump to adjust its output current level so that the product of the measured gain and a charge pump current level is kept constant.

19. The phase-locked loop circuit as claimed in claim 17, further comprising:

a voltage reference circuit, operatively connected to said programmable charge pump and said analog to digital converter, to generate and apply a same reference voltage to said programmable charge pump and said analog to digital converter based upon changes in a bandgap voltage.

20. The phase-locked loop circuit as claimed in claim 16, further comprising:

an integer-N divider operatively connected to an output of said oscillator; and

a phase and frequency detector operatively connected between said integer-N divider and said programmable charge pump.

21. The phase-locked loop circuit as claimed in claim 20, wherein said control loop controls said programmable charge circuit to adjust its output current level so that the product of the measured gain and a charge pump current level divided by an average N value, said N value being provided by said integer-N divider, is kept constant.

22. The phase-locked loop circuit as claimed in claim 16, further comprising:

a programmable gain amplifier to receive either a signal from a calibration signal;

a comparator for comparing a voltage of an output from said programmable gain amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator to produce a gain signal; and

a gain controller, in response to said gain signal produced by said comparator, to control a gain of said programmable gain amplifier.

23. The phase-locked loop circuit as claimed in claim 22, wherein said gain controller includes a counter and a plurality of resistors, said plurality of resistors being switchable into or out of a circuit connected between an output of said programmable gain amplifier and an input of said programmable gain amplifier.

24. The phase-locked loop bandwidth calibration circuit as claimed in claim 22, wherein said gain controller controls the gain of said programmable gain amplifier such that a full scale input to said programmable gain amplifier produces said predetermined frequency shift in said oscillator.

25. The phase-locked loop circuit as claimed in claim 16, wherein said phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said capacitor to a voltage of said phase-locked loop filter; and a switch to switch said capacitor into the phase-locked loop filter circuit to effect a phase-locked loop bandwidth.

26. The phase-locked loop circuit as claimed in claim 16, wherein said phase-locked loop filter includes a dual path having an integrator path and a lead-lag path.

27. A method of calibrating a phase-locked loop bandwidth, comprising:

(a) setting a phase-locked loop at a local oscillator offset;

(b) allowing the phase-locked loop to settle;

(c) measuring a first gain of a voltage-controlled oscillator located in the phase-locked loop;

(d) setting the phase-locked loop to a channel center frequency;

(e) allowing the phase-locked loop to settle;

(f) measuring a second gain of the voltage-controlled oscillator;

(g) determining a difference between the first and second gain measurements; and

(h) controlling a programmable charge circuit located in the phase-locked loop to adjust its output current level based on the determined gain difference.

28. The method as claimed in claim 27, wherein the programmable charge circuit adjusts its output current level so that the product of a measured gain and a charge pump current level is kept constant.

29. A system for processing received radio-frequency signals, comprising:

a receiver to receive the radio-frequency signals;

a mixing unit to mix down the received radio-frequency signals to baseband;

a frequency synthesizer to generate signals used by said mixing unit in mixing down the received radio-frequency signals to baseband;

a filtering unit to lowpass filter the baseband radio-frequency signals; and

a RC calibration unit to determine R and C values of said filtering unit so as to calibrate pole & zero frequencies of said filtering unit;

said frequency synthesizer including a phase-locked loop circuit having a programmable charge pump, a phase-locked loop filter operatively connected to said programmable charge pump, and an oscillator, operatively connected to said phase-locked loop filter, to generate a frequency signal based upon a signal received from said phase-locked loop filter;

said RC calibration unit using said determined R and C values to calibrate pole & zero frequencies of said phase-locked loop filter.

30. The system as claimed in claim 29, further comprising:

a control loop operatively connected to said phase-locked loop filter and said programmable charge pump;

said control loop controlling said programmable charge pump to adjust its output current level based on a measured gain of said oscillator.

31. The system as claimed in claim 30, wherein said control loop includes a voltage measurement circuit, operatively connected to said phase-locked loop filter, to measure a voltage being output from said phase-locked loop filter; an analog to digital converter, operatively connected to said voltage measurement circuit, to convert the measured voltage into a digital signal; and a controller to cause said programmable charge pump to adjust its output current level based upon a received digital signal from said analog to digital converter.

32. The system as claimed in claim 30, wherein said control loop controls said programmable charge pump to adjust its output current level so that the product of the measured gain and a charge pump current level is kept constant.

33. The system as claimed in claim 31, further comprising:

a voltage reference circuit, operatively connected to said programmable charge pump and said analog to digital converter, to generate and apply a same reference voltage to said programmable charge pump and said analog to digital converter based upon changes in a bandgap voltage.

34. The system as claimed in claim 30, further comprising:

an integer-N divider operatively connected to an output of said oscillator; and

a phase and frequency detector operatively connected between said integer-N divider and said programmable charge pump.

35. The system as claimed in claim 30, further comprising:

a programmable gain amplifier to receive either a signal from a calibration signal;

a comparator for comparing a voltage of an output from said programmable gain amplifier with a voltage necessary to produce a predetermined frequency shift in said oscillator to produce a gain signal; and

a gain controller, in response to said gain signal produced by said comparator, to control a gain of said programmable gain amplifier.

36. The system as claimed in claim 30, wherein said phase-locked loop filter includes a capacitor; a charging circuit to pre-charge said capacitor to a voltage of said phase-locked loop filter; and a switch to switch said capacitor into the phase-locked loop filter circuit to effect a phase-locked loop bandwidth.

37. The system as claimed in claim 30, wherein said phase-locked loop filter includes a dual path having an integrator path and a lead-lag path.

38. The system as claimed in claim 29, wherein said programmable charge pump has a resistive value; said phase-locked loop filter has a resistive value; and said resistive value of said programmable charge pump is matched to said resistive value of said phase-locked loop filter.

39. The system as claimed in claim 30, wherein said programmable charge pump has a resistive value; said phase-locked loop filter has a resistive value; and said resistive value of said programmable charge pump is matched to said resistive value of said phase-locked loop filter.